**Field Effect Transistors**

**JFETs (Junction Field Effect Transistors)**

Although there are lots of confusing names for field effect transistors (FETs) there are basically two main types:

1. The reverse biased PN junction types, the JFET or Junction FET, (also called the JUGFET or Junction Unipolar Gate FET).

2. The insulated gate FET devices (IGFET).

All FETs can be called UNIPOLAR devices because the charge carriers that carry the current through the device are all of the same type i.e. either holes or electrons, but not both. This distinguishes FETs from the bipolar devices in which both holes and electrons are responsible for current flow in any one device.

**The JFET**

This was the earliest FET device available. It is a voltage−controlled device in which current flows from the SOURCE terminal (equivalent to the emitter in a bipolar transistor) to the DRAIN (equivalent to the collector). A voltage applied between the source terminal and a GATE terminal (equivalent to the base) is used to control the source − drain current. The main difference between a JFET and a bipolar transistor is that in a JFET no gate current flows, the current through the device is controlled by an electric field, hence "Field effect transistor". The JFET construction and circuit symbols are shown in Figures 1, 2 and 3.

**JFET Construction**

The construction of JFETs can be theoretically quite simple, but in reality difficult, requiring very pure materials and clean room techniques. JFETs are made in different forms, some being made as discrete (single) components and others, using [planar technology](http://www.learnabout-electronics.org/bipolar_junction_transistors_03.php) as integrated circuits.

**Fig.1.1 Diffusion JFET Construction**

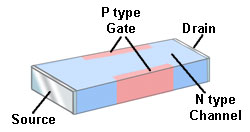


Fig. 1.1 shows the (theoretically) simplest form of construction for a Junction FET (JFET) using diffusion techniques. It uses a small slab of N type semiconductor into which are infused two P type areas to form the Gate. Current (electrons) flows through the device from source to drain along the N type silicon channel. As only one type of charge carrier (electrons) carry current in N channel JFETs, these transistors are also called "Unipolar" devices.

**Fig. 1.2 JFET Planar Construction**

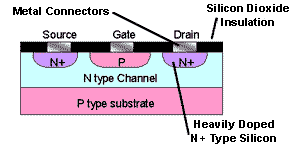
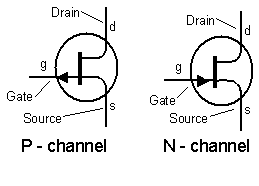


Fig. 1.2 shows the cross section of a N channel planar Junction FET (JFET) The load current flows through the device from source to drain along a channel made of N type silicon. In the planar device the second part of the gate is formed by the P type substrate.

P channel JFETs are also available and the principle of operation is the same as the N channel type described here, but polarities of the voltages are of course reversed, and the charge carriers are holes.

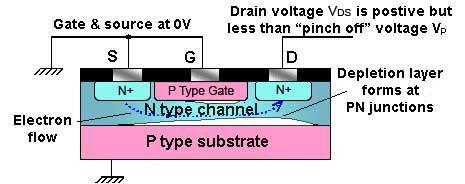
**Fig. 1.3 JFET Circuit symbols**



**How a JFET Works.**

**The JFET is a Voltage Operated Transistor.**

**Fig. 2.1 JFET Operation Below "Pinch Off".**

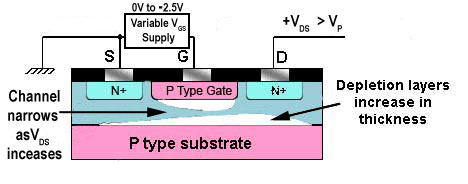


In the N channel device, the N channel is sandwiched between two P type regions (the gate and the substrate) that are connected together electrically to form the gate. The N type channel is connected to the source and drain terminals via more heavily doped N+ type regions. The drain ic connected to a positive supply, and the source to zero volts. N+ type silicon has a lower [resistivity](http://www.learnabout-electronics.org/resistors_04.php) than N type. This gives it a lower resistance, increasing conduction and reducing the effect of placing standard N type silicon next to the aluminium connector, which because aluminium is a tri−valent material, having three valence electrons whilst silicon has four, would tend to create an unwanted junction, similar in effect to a PN junction at this point.

The P type gate is at 0V and is therefore negatively biased compared to the channel, which has a potential gradient on it, as one end is connected to 0 volts (the source), and the other end to a positive voltage (the drain). Any point on the channel (apart from the extreme end near the source terminal) must therefore be more positive than the gate. Therefore the two PN junctions formed between the N type channel and the P type areas of the gate and the substrate are both reverse biased, and so have a depletion layer that extends into the channel as shown in Fig. 2.1.

The shape of the depletion layer is not symmetrical, as can be seen from Fig. 2.1. It is generally thicker towards the drain end of the channel, because the voltage on the drain is more positive than that on the source due to voltage gradient that exists along the channel. This causes a larger potential across the junctions nearer the drain, and so a thickening of the depletion layer. The effect becomes more marked when the voltage between drain and source is greater than about 1volt or so.

**Fig. 2.2 JFET Operation Above "Pinch Off"**

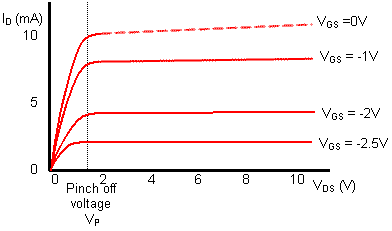


When a voltage is applied between drain and source (VDS) current flows and the silicon channel acts rather like a conventional resistor. Now if VDS is increased (with VGS held at zero volts) towards what is called the pinch off value VP, the drain current ID also at first, increases. The transistor is working in the "ohmic region" as shown in Fig. 2.1.

However as drain source voltage VDS increases, the depletion layers at the gate junctions are also becoming thicker and so narrowing the N type channel available for conduction. There comes a point, known as "pinch off" where the conducting channel has become narrow enough to cancel out the effect of current increasing with the applied voltage VDS as shown in fig 2.2. Above this point there is little further increase in drain current and the transitor is said to operating in "saturation mode". With the JFET biased in this way, a small change in VGS can be used to control the current through the source−drain channel from its maximum(saturated) value to zero current.

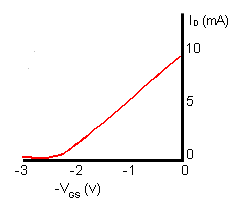
This type of operation is shown in the fairly flat top to the output characteristics shown in fig 2.3. Notice that each curve is drawn for a particular value of negative voltage between gate and source, and that when sufficient reverse bias is applied to the gate (e.g. more than −2.5V, the lowest value on the graph) the drain current ceases completely.

**Fig. 2.3 JFET Output Characteristic**



In the JFET output characteristics shown in Fig. 2.3, the Drain current ID shows very little change, and the curves are very nearly horizontal at voltages greater than the pinch off voltage. Almost all of the expected increase in current, due to the increase in voltage between Source and Drain (VDS), is offset by the narrowing of the conducting channel due to the growing depletion layers.

**Fig. 2.4 JFET Transfer Characteristic**



The transfer characteristic for a JFET, which shows the change in Drain current (ID) for a given change in Gate−Source voltage (VGS), is shown in Fig 2.4. Because the JFET input (the Gate) is voltage operated, the gain of the transistor cannot be called current gain, as with bipolar transistors. The drain **current** is controlled by the Gate−Source **voltage**, so the graph shows milliamperes per volt (mA / V), and as I / V is CONDUCTANCE (the inverse of resistance V / I) the slope of this graph (the gain of the device) is called the FORWARD or MUTUAL TRANSCONDUCTANCE, which has the symbol gm. Therefore the higher the value of gm the greater the amplification.

Notice that VGS is always shown as being negative; in reality it may be zero or slightly above zero, but the gate is always more negative than the N type channel between source and drain. Note also that the slope of the curve in the transfer characteristic is less steep than that of the transfer characteristic for a typical bipolar transistor . This means that a JFET will have a lower gain than that of a bipolar transistor.

This disadvantage is offset by the advantage of having an extremely high input resistance. A typical input resistance for a JFET would be in the region of 1 x 1010 ohms (10,000 Megohms!) compared with 2K to 3K Ohms for a bipolar device.

This makes the JFET ideal for applications where the circuit or device driving the JFET amplifier cannot supply any appreciable current, an example being the Electret microphone, which uses a FET within the microphone to amplify the tiny voltage variations appearing across the vibrating diaphragm element.

Another feature of the JFET that makes it more suited to very high frequency use than bipolar transistors, is the absence of junctions in the JFET conducting channel. In a bipolar transistor two PN junctions forming tiny capacitances, exist between base and emitter, and base and collector, due to the PN junctions. These capacitances will limit high frequency performance, as they provide negative feedback paths at high frequencies. Because the JFET is in effect just a slab of silicon between Source and Drain, the stray capacitances that exist in bipolar devices are absent, so high frequency performance is improved, making JFETs usable even at hundreds of MHz

**Enhancement Mode MOSFET**

**The Insulated Gate FET (IGFET).**

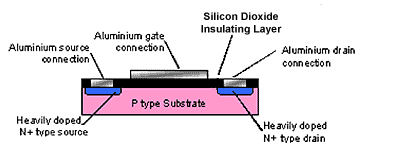
The Metal Oxide Silicon FET (MOSFET) or Metal Oxide Silicon Transistor (M.O.S.T.) has an even higher input resistance (typically 1012 to 1015 ohms) than that of the JFET. In the MOSFET device the gate is completely insulated from the rest of the transistor by a very thin layer of metal oxide (Silicon dioxide SiO2). Hence the general name applied to any device of this type, is the IGFET or Insulated Gate FET.

**Planar Technology.**

There are several ways in which an insulated gate transistor may be constructed. All the methods used however, make use of planar technology in which the various parts of the device are laid down as planes or layers on the upper surface of a "SUBSTRATE" in a similar way to that shown on the [Planar Transistors](http://www.learnabout-electronics.org/bipolar_junction_transistors_03.php) page in the BJT section.

The layers are laid down one by one, by diffusing various semiconductor materials with suitable doping levels, as well as layers of insulation into the surface of the device, under carefully controlled conditions at high temperatures. Parts of a layer may be removed by etching, using photographic masks to make the required pattern of the electrodes etc. before the next layer is added. The insulating layers are made by laying down very thin layers of silicon dioxide and conductors are created by evaporating a metal, such as aluminium on to the surface. The transistors produced in this way have a much higher quality than is possible using other methods, and many transistors can be produced at one time on a single slice of silicon, before the silicon slice is cut up into individual transistors or integrated circuits.

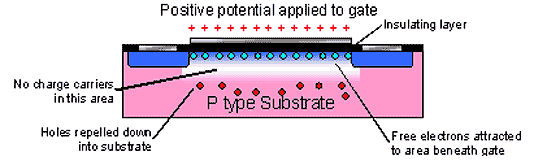
**Fig. 4.1 Construction of a N Channel Enhancement Mode MOSFET**



The basic construction of a MOSFET is shown in Fig. 4.1. A body or substrate of P type silicon is used, then two heavily doped N type regions are diffused into the upper surface, to form a pair of closely spaced strips.

A very thin (about 10−4 mm) layer of silicon dioxide is then evaporated onto the top surface forming an insulating layer. Parts of this layer are then etched away above the N type regions using a photographic mask to leave these regions uncovered. On top of the insulating layer, between the two N type regions, a layer of aluminium is deposited. This acts as the GATE electrode. Metal contacts are also deposited on the N type regions, which act as the SOURCE and DRAIN connectors

**Fig 4.2 Enhancement Mode Operation.**



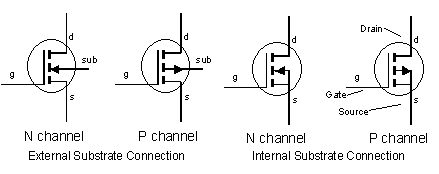
The gate has a voltage applied to it that makes it positive with respect to the source. This causes holes in the P type layer close to the silicon dioxide layer beneath the gate to be repelled down into the P type substrate, and at the same time this positive potential on the gate attracts free electrons from the surrounding substrate material. These free electrons form a thin layer of charge carriers beneath the gate electrode (they can't reach the gate because of the insulating silicon dioxide layer) bridging the gap between the heavily doped source and drain areas. This layer is sometimes called an "inversion layer" because applying the gate voltage has caused the P type material immediately under the gate to firstly become "intrinsic" (with hardly any charge carriers) and then an N type layer within the P type substrate.

Any further increase in the gate voltage attracts more charge carriers into the inversion layer, so reducing its resistance, and increasing current flow between source and drain. Reducing the gate source voltage reduces current flow. When the power is switched off, the area beneath the gate reverts to P type once more.

As well as the type described above, devices having N type substrates and P type (inversion layer) channels are also available. Operation is identical, but of course the polarity of the gate voltage is reversed.

This method of operation is called "ENHANCEMENT MODE" as the application of gate source voltage makes a conducting channel "grow", therefore it enhances the channel. Other devices are available in which the application of a bias voltage reduces or "depletes" the conducting channel.

**Fig. 4.3 Circuit Symbols for Enhancement Mode MOSFETs (IGFETs)**



**Handling Precautions.**

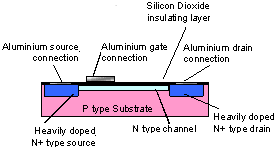
In operation, although the gate has a voltage applied to it, no gate current flows because of the silicon dioxide layer beneath the gate terminal. One well known problem exists regarding this layer however. Although silicon dioxide is an excellent insulator, the layer used on a MOSFET is extremely thin, and therefore can be permanently damaged if a high voltage is applied across it. It will break down just as any other insulator will. Because it is so very thin, it does not need very high voltages to cause total breakdown, and as the gate has such a very high resistance, any voltage present will not be reduced by current flow.

Therefore voltages due to static electricity, which are present all the time in almost any environment, and may reach several thousand volts if no current is drawn to discharge them, present a threat to the insulating layer. For this reason it is wise to transport FETs in special conductive packaging so that no voltage can build up between any of the terminals of the device. Once the transistor is connected into a circuit, the components of the circuit should afford sufficient protection by forming conducting paths around the device, so preventing the build up of high static voltages. In most modern devices special protection diodes are built in to the device to give some protection against static damage. This protection is limited however, and manufacturers handling instructions should be studied before handling any MOS device.

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**Depletion Mode MOSFET**

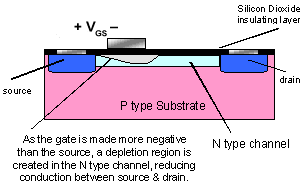
**Fig 5.1 Depletion Mode N Channel MOSFET**



The depletion mode MOSFET shown as a N channel device (P channel is also available) in Fig 5.1 is more usually made as a discrete component, i.e. a single transistor rather than IC form. In this device a thin layer of N type silicon is deposited just below the gate−insulating layer, and forms a conducting channel between source and drain.

Therefore when the gate source voltage VGS is zero, current (in the form of free electrons) can flow between source and drain. Note that the gate is totally insulated from the channel by the layer of silicon dioxide. Now that a conducting channel is present the gate does not need to cover the full width between source and drain. Because the gate is totally insulated from the rest of the transistor this device, like other IGFETs, has a very high input resistance.

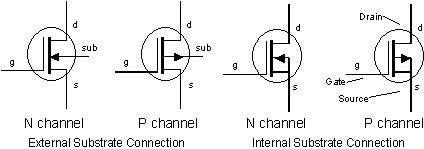
**Fig. 5.2 Operation of a Depletion Mode MOSFET**



In the N channel device, shown in Fig. 5.2 the gate is made negative with respect to the source, which has the effect of creating a depletion area, free from charge carriers, beneath the gate. This restricts the depth of the conducting channel, so increasing channel resistance and reducing current flow through the device.

Depletion mode MOSFETS are also available in which the gate extends the full width of the channel (from source to drain). In this case it is also possible to operate the transistor in enhancement mode. This is done by making the gate positive instead of negative. The positive voltage on the gate attracts more free electrons into the conducing channel, while at the same time repelling holes down into the P type substrate. The more positive the gate potential, the deeper, and lower resistance is the channel. Increasing positive bias therefore increases current flow. This useful depletion/enhancement version has the disadvantage that, as the gate area is increased, the gate capacitance is also larger than true depletion types. This can present difficulties at higher frequencies.

**Fig. 5.3 Circuit Symbols for Depletion Mode MOSFETs (IGFETs)**



Notice the solid bar between source and drain, indicating the presence of a conducting channel.

Note: Making the gate more negative reduces conduction between source & drain In N channel devices, but increases conduction between source & drain In P channel devices.

**Applications of FETs**

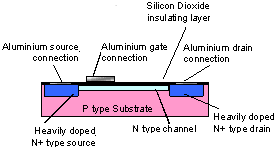
Although FETs have a lower gain than bipolar transistors, their very high input impedance makes them suitable for applications where input signals may be severely reduced if applied to a bipolar transistor base that needs base current to operate. The planar technology used to make FETs is the same as that used to make integrated circuits, so most of the transistors found in I / Cs are of this type. A useful feature of FETs is that they tend to produce less background noise than Bipolar types and so are useful in the initial stages of systems such as amplifiers; radios etc. where signal levels are very small and could be swamped by excessive background noise.

**High Power FETs**

FETs used in high power output stages are often seen referred to as VMOS, DMOS or TMOS. These transistors are basically the same as other IGFETs but have specialised constructions that allow them to pass currents as large as 10A. They are also able to switch on and off very quickly (in nano seconds). This allows them to be used in such circuits as switch mode power supplies where very fast switching is essential.

**Depletion Mode MOSFET**

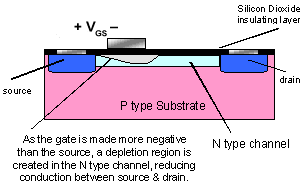
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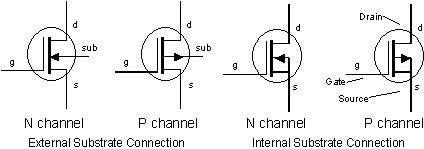
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